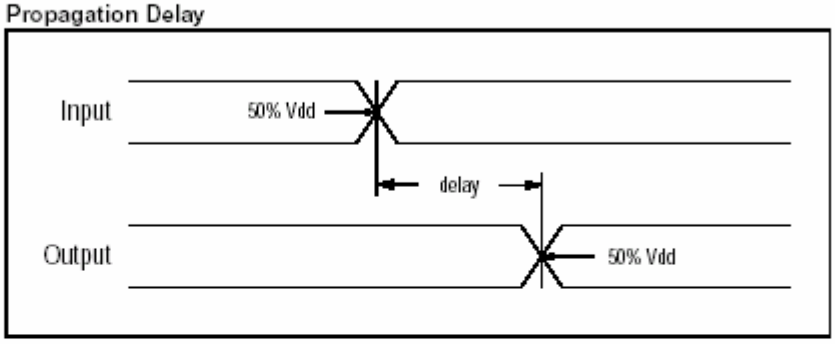
TIMING PARAMETERS DEFINITION

Propagation Delay

The propagation delay through a cell is the sum of the intrinsic delay, the load-dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing 50% of Vdd and the output crossing 50% of Vdd. The following diagram illustrates propagation delay.

Propagation Delay



Factors that affect propagation delays include: temperature, supply voltage, process variations, fanout loading, interconnect loading, input-transition time, input-signal polarity, and timing constraints (see below). The timing models provided with this library include the effects of input-transition time on propagation delays. Also, all timing models use a table lookup method to calculate accurate timing. To simplify calculations, the standard cell datasheets provide all timing numbers for an input slew of 0.05ns and a linearized load factor, K_{load}, which is not as accurate as the timing models. All cells have been characterized with a fully populated metal2 (0.9µm horizontal pitch) and metal3 (0.8µm vertical pitch) routing grid across the entire cell layout.

The SAGE Standard Cell Library may contain negative propagation delays. Although most third-party verification tools can handle negative propagation delays, some tools will turn negative delays into a zero value.

Delay Calculation

Using the delay data in the datasheets ($t_{intrinsic}$, K_{load}, and C_{load}) and the delay derating factors, the estimated total propagation delay is

$$t_{TPD} = (K_{Process}) \bullet [1+(K_{Volt} \bullet \Delta Vdd)] \bullet [1+(K_{Temp} \bullet \Delta T)] \bullet t_{typical}$$

$$t_{typical} = t_{intrinsic} + (K_{load} \bullet C_{load})$$

where

t_{TPD} = total propagation delay (ns);

$t_{typical}$ = delay at typical corner—2.5V, 25°C, typical process (ns);

$t_{intrinsic}$ = delay through the cell when there is no output load (ns);

K_{load} = load delay multiplier (ns/pF);

C_{load} = total output load capacitance (pF);

$K_{Process}$ = process derating factor, where process is slow, typical, or fast;

K_{Volt} = voltage derating factor (/V);

ΔVdd = Vdd - 2.5V;

K_{Temp} = temperature derating factor (/°C);

ΔT = junction temperature - 25°C.

Timing Constraints

Timing constraints define minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing constraints include: setup time, hold time, recovery time, and minimum pulse width.

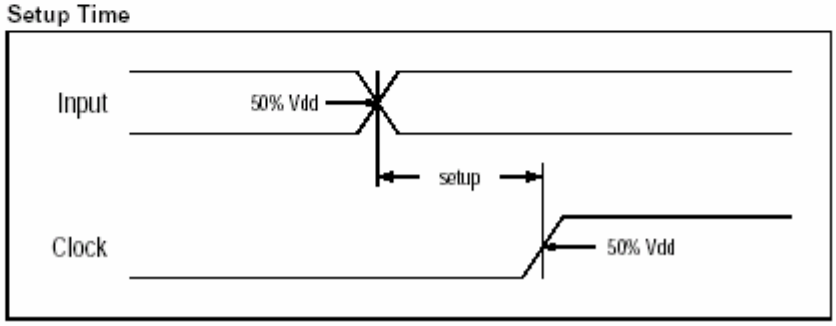
The sequential-cell timing models provided with this library include the effects of input-transition time and data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for 0.05ns data slew and 0.05ns clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process case variations. All cells have been characterized with a fully populated metal2 (0.9µm horizontal pitch) and metal3 (0.8µm vertical pitch) routing grid across the entire cell layout.

Timing constraints can affect propagation delays. The intrinsic delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, and pulse widths). The use of shorter timing constraint intervals may increase delay. Each cell is considered functional as long as the actual delay does not exceed the delay given in the datasheets by more than 10%.

Setup Time

The setup time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%. Setup-constraint values are measured as the interval between the data signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd. For the measurement of setup time, the data input signal is kept stable after the active clock edge for an infinite hold time. The following diagram illustrates setup time for a positive-edge-triggered sequential cell.

Setup Time

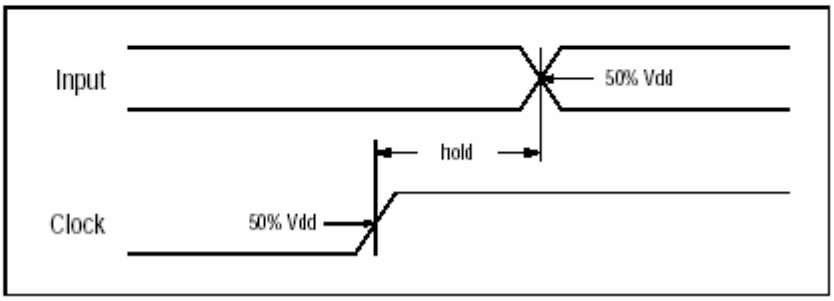


Hold Time

The hold time for a sequential cell is the minimum length of time the data-input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%. Hold-

constraint values are measured as the interval between the clock signal crossing 50% of Vdd and the data signal crossing 50% of Vdd. For the measurement of hold time, the data input signal is held stable before the active clock edge for an infinite setup time. The following diagram illustrates hold time for a positive-edge-triggered sequential cell.

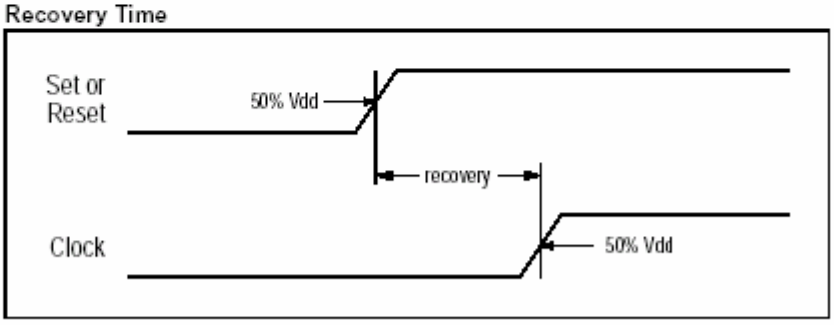
Hold Time



Recovery Time

Recovery time for sequential cells is the minimum length of time that the active-low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd. For the measurement of recovery time, the set or reset signal is held stable after the active clock edge for an infinite hold time. The following diagram illustrates recovery time.

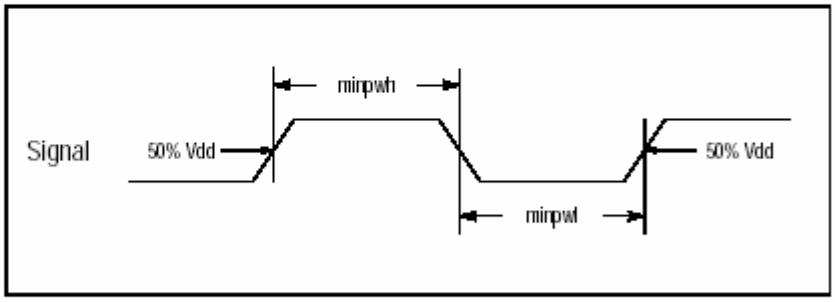
Recovery Time



Minimum Pulse Width

Minimum pulse width is the minimum length of time between the leading and trailing edges of a pulse waveform. Minimum pulse width high (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of Vdd and the falling edge of the signal crossing 50% of Vdd. Minimum pulse width low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of Vdd and the rising edge of the signal crossing 50% of Vdd. The following diagram illustrates minimum pulse width.

Minimum Pulse Width



Minimum pulse width is defined to be 0.81ns for all set/reset pins (SN, RN) and 0.31ns for all clock pins (G, GN, CK, CKN). These are the largest minimum pulse widths measured from all the cells in the library. An input pulse of shorter duration will produce unpredictable results.

Power Calculation

Power dissipation is dependent upon the power-supply voltage, frequency of operation, internal capacitance, and output load. The power dissipated by each cell is

$$P_{avg} = \sum_{n=1}^{x} (E_{in} \bullet f_{in}) + \sum_{n=1}^{y} \left(C_{on} \bullet Vdd^2 \bullet \frac{1}{2} f_{on} \right) + E_{os} \bullet f_{o1}$$

where

P_{avg} = average power (µW);

x = number of input pins;

E_{in} = energy associated with the nth input pin (µW/MHz);

f_{in} = frequency at which the nth input pin changes state during the normal operation of the design (MHz);

y = number of output pins;

C_{on} = external capacitive loading on the nth output pin, including the capacitance of each input pin connected to the output driver, plus the route wire capacitance, actual or estimated (pF);

Vdd = operating voltage = 2.5V;

f_{on} = frequency at which the nth output pin changes state during the normal operation of the design (MHz);

E_{os} = energy associated with the output pin for sequential cells only (µW/MHz).

The switching frequency of inputs and outputs of a particular cell in a design can be obtained from a gate-level logic simulator, for example Verilog, by applying typical input stimuli and measuring the activity on each node of interest. The total average power for the design can be computed by adding the average power for each cell.

For example, for a DFFXL cell with clock switching at 133MHz, input and output pins switching at 20MHz, an external capacitive loading on the output pin of 0.02pF, and using the power table in the DFF datasheet shown on page 24, the power dissipated by the DFFXL is given by the equation:

$$P_{avg} = \sum_{n=1}^{x} (E_{in} \bullet f_{in}) + \sum_{n=1}^{y} \left(C_{on} \bullet Vdd^2 \bullet \frac{1}{2} f_{on} \right) + E_{os} \bullet f_{o1}$$