Evolutionary Synthesis of Fuzzy Circuits

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Abstract

Recent research in evolutionary synthesis of electronic circuits and evolvable hardware [1], [2] has generated a set of ideas and demonstrated a set of concepts that have direct application to the computational circuits used for information processing in fuzzy systems.

This paper overviews five such concepts developed by the author: 1) evolutionary techniques for automatic synthesis of electronic circuits implementing fuzzy operators and functions, 2) re-configurable devices for fuzzy configurable computing and on-chip evolution of fuzzy systems, 3) mixtrinsic evolution for automatic modeling/identification of correlated fuzzy models of different granularity/resolution/flavor, 4) accelerating circuit evolution (and modeling in general) through gradual morphing through fuzzy topologies, and 5) polymorphic electronics as circuits with superimposed multiple functionality, in particular fuzzy functionality.

1) Evolutionary synthesis of electronic circuits for fuzzy systems

Evolutionary algorithms (EA) have proven to be powerful search mechanisms able to automatically find novel circuits/topologies that satisfy desired functional and implementation/efficiency-related requirements. In particular EA can be applied to determine circuits that implement operators such as conjunctions and disjunctions modeled by triangular norms, which is a central element for fuzzy systems.

While circuits implementing simple t-norms/co-norms, such as min, max, product and probabilistic sum, have been explored quite early, more complex t-norms, such as parametric t-norms (e.g. Frank's t-norms explored in [3]), while shown valuable both in theoretical studies as well as in practical applications (such as in the fuzzy controllers by Gupta et al in FSS in early 90s, see [4], [5]) are still lacking circuit solutions. The reasons are simple: such circuits (referring here to analog circuits – computing the functions digitally or storing tables in memory being computationally expensive solutions in terms of power/time/area of silicon) are hard to design – each would practically mean a new patent, and one may need many of them, one for each value of the parameter of the t-norm (unless of course one designs a parametric circuit, which would be an even harder task).

Evolutionary techniques have proven efficiency (and proficiency) in creating such new designs for implementation of parametric t-norm circuits. Several such circuits are presented in [6] and will be shown for illustration. See Figures 1, 2 and 3 for exemplification (Figure 1 shows the FPTA cell discussed in the next section).

2) Re-configurable/evolvable devices for fuzzy configurable computing

The Field Programmable Transistor Arrays (FPTA)[7], [8] are devices on which one can program circuits at the lowest granularity and achieve the highest control of the topology, i.e. by reconfiguration at the transistor level. These devices were conceived as platforms for rapid experiments in evolutionary synthesis; instead of simulating circuits (and in fact very many of them, as required by EA), one would just instantiate them on the configurable chips and evaluate the measured response. (Evolutionary design could benefit from various models of different granularity, sub-circuits of several transistors can be "frozen" and used as components of higher level of granularity. For various levels of modeling, evolvability and granularity levels see [9]).

First, from the perspective of fuzzy computational platforms, these devices are versatile/malleable architectures on which one can rapidly instantiate the desired fuzzy circuitry. Second, these are adaptable and can be used to implement systems that change the operators from one processing stage to the other, i.e. one can start with MIN-MAX logic and change later to another as needed. Third, the FPTA are platforms for fuzzy configurable computing in the same way FPGAs are for conventional/digital computing. In an ASIC version the whole processing described by an algorithm is mapped at once in a fixed circuitry, with building blocks corresponding to various stages of the algorithm. In an FPGA/FPTA implementation, only a part of the algorithm is mapped first in an instance of the processing machine, after which the chip reconfigures itself to become the blueprint for the next step, and so on. The fourth aspect is related to the use of FPTA to evolve fuzzy circuits directly in hardware. This not only is rapid, but also real, i.e. valid without doubts, unlike the case of evolution in simulations which may lead to results that may differ when tested in reality due to modeling approximation and fabrication effects. In other words evolution on real chips takes in consideration and adapts to account for effects of fabrication, temperature of operation, etc.

3) Mixtrinsic evolution

Several fuzzy researchers, foremost Prof. Zadeh, emphasize the importance of concepts such as information granularity and processing of information at different levels of granularity. In complex electronic systems, to cope with the complexity induced by explosion in number of components reflected by Moore's Law, and also recently the extra challenges related to systems-on-a-chip – the idea of using high-level approaches (models, languages) imposes as an undisputable necessity. One needs however to preserve the connection to and representation power for the structures below – at finest levels of granularity/resolution. Thus, models of different complexity are needed for given entity. Mixtrinsic evolution (introduced in [10]) is a method of modeling (model construction and identification) which allows simultaneous development of

coherent/corresponding models. Traditional modeling uses one model type only. In evolutionary modeling a population of same-type models is evaluated. For example, in evolving electronic circuits on FPTA - in simulations - one can use a resistive model for the interconnecting switches. Alternatively one can use the more realistic model for the switch, considering two back-to-back transistors. The two circuits simulate at different speeds, the resistive one much faster, while less accurate. The problem is that evolving solutions using only one representation one may result in (and this has been shown in practice in various contexts) "solutions" (characterized in first instance by a genetic code that from which the circuit is derived) that do not work in the context of the other representation, e.g. a. derived model obtained using resistive switches may not work when tested on the transistor-based representation, and viceversa.

The idea of mixtrinsic evolution is to have a mixed population in which candidate solutions may be at different levels of resolution (or perhaps even of very different nature). One approach is to assign the solutions (which in evolutionary design model are coded in chromosomes) to alternative instantiations of different resolution changing from a generation to another. Another approach is to have a combined fitness function that characterizes the modeling ensemble (i.e. each candidate solution in all its instantiations at different levels of resolution). Both approaches were demonstrated to werk, illustrated on problems on which not applying the method results in solutions that are not equivalent at different levels of resolution. (In some other experiments we used SW models and HW programmed circuits and converged to solutions with similar behaviors).

4) Gradual morphing through fuzzy topologies

The idea comes from early experiments with the FPTA. Switches interconnecting transistors are not ON/OFF but can be controlled gradually with analog voltages on the gates of transistors that make the switch. In current implementation analog Low and High sighnals are the same for all switches on the chip. This allows to map the 1/0-based genetic code/program of the switch to a Low/High resistance, not only to ON/OFF (i.e. very low, and very high), but to a great number of in-between values. Thus, the switches can be partly-open, allowing the signals to more freely propagate/spread over the topology. The basic idea behind the technique that accelerate evolution compared to the case when the search proceeds only with ON/OFF status, is inspired from annealing.
A temperature parameter is high at the beginning of evolution and decreasing to null over generations. When it is "hot" there is a lot of "thermal movement" and the Low/High values for the resistance of the switch, are close to each other, somewhere in the middle range (say 2k/10k). As the temperature decreases the two separate, low becoming lower, high becoming higer (e.g. (1k/30k), (500/100k) ending up for example at (5/100M). This annealing was demonstrated to accelerate evolution, in some experiments over 10 times [11]. When we operate on a physical FPTA chip we could stop evolution early, since solutions usually show up in the first few generations and are fully operational. If the interest is to evolve a design that would go on an ASIC (or a circuit to be patented, where either there are, or there are no connections between components) then evolution has to maintain the acquired solution while "cooling" to ON/OFF connectivity.

The gradual opening seems to permit signal propagation to points where OFF switches in a traditional ON/OFF Boolean search may prevent it, making it more a "needle in-the-hay" search problem. Another way of looking at the circuits connected by gradual switches is to see not one, but several superimposed (conventional/Boolean) topologies at once –a fuzzy topology. These superposition/fuzziness allows for a more parallel search.

5) Polymorphic electronics

Polymorphic electronics (polytronics) is a new category of electronic circuits with superimposed built-in functionality. A function change does not require switches/reconfiguration as in traditional approaches. Instead, the change comes from modifications in the characteristics of devices involved in the circuit, in response to controls such as temperature, power supply voltage (VDD), control signals, light, etc. For example, a temperature-controlled polytronic AND/OR gate behaves as AND at 27C and as OR at 125C. Polytronic circuits in which the control is by temperature, morphing signals, and VDD respectively are demonstrated in [12]. Polymorhic circuits were synthesized by evolutionary design/evolvable hardware techniques. These techniques are ideal for the polytronics design, a new area that lacks design guidelines/know-how,- yet the requirements/objectives are easy to specify and test. The circuits are evolved/synthesized in two different modes. The first mode explores an unstructured space, in which transistors can be interconnected freely in any arrangement (in simulations only). The second mode uses the FPTA model, and the circuit topology is sought as a mapping onto a programmable architecture (these experiments were performed both in simulations and on FPTA chips). The experiments demonstrate the polytronics concept and the synthesis of polytronic circuits by evolution. The capacity of storing/hiding "extra" functions provides for watermark/invisible functionality, thus polytronics may find uses in intelligence/security applications. Built-in environment-reactive behavior (e.g. changing function with temperature) may also find uses in a variety of space and military applications. From the perspective of fuzzy systems, one can think of polymorphic fuzzy circuits, i.e. circuits with superimposed fuzzy functions.

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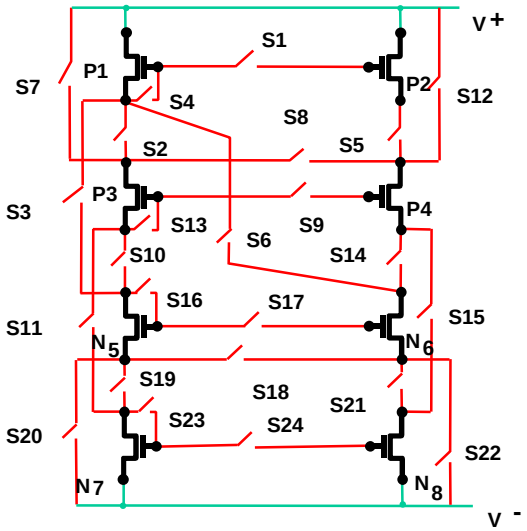

Figure 1 FPTA cell consisting of 8 transistors and 24 programmable switches.

The family of Frank T- norms is given by

$$T_s(x,y) = \begin{cases} \text{MIN}(x,y) & \text{if } (s = 0) \\ x \cdot y & \text{if } (s = 1) \\ \log_s\left[1 + \dfrac{(s^x - 1).(s^y - 1)}{s - 1}\right] & \text{if } (0 < s < \infty),\ s \neq 1 \\ \text{MAX}(0, x + y - 1) & \text{if } (s = \infty) \end{cases} \quad (1)$$

The family of Frank T-conorms is given by

$$S_s(x,y) = \begin{cases} \text{MAX}(x,y) & \text{if } (s = 0) \\ x + y - x.y & \text{if } (s = 1) \\ 1 - \log_s\left[1 + \dfrac{(s^{1-x} - 1).(s^{1-y} - 1)}{s - 1}\right] & \text{if } ((0 < s < \infty),\ s \neq 1) \\ \text{MIN}(1, x + y) & \text{if } (s = \infty) \end{cases} \quad (2)$$

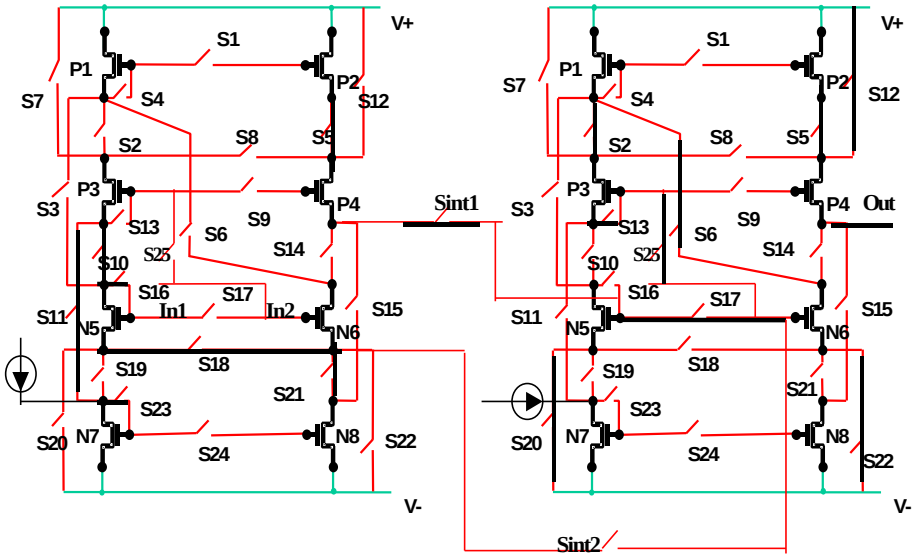

Figure 2 Evolved circuit implementing the fundamental T-norm for s=100 (with the response in Figure 3).

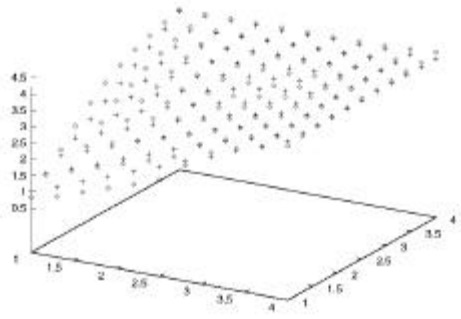

Figure 3 Response of a circuit implementing the fundamental S-norm for s=100 (◊). Target characteristic shown with (+).

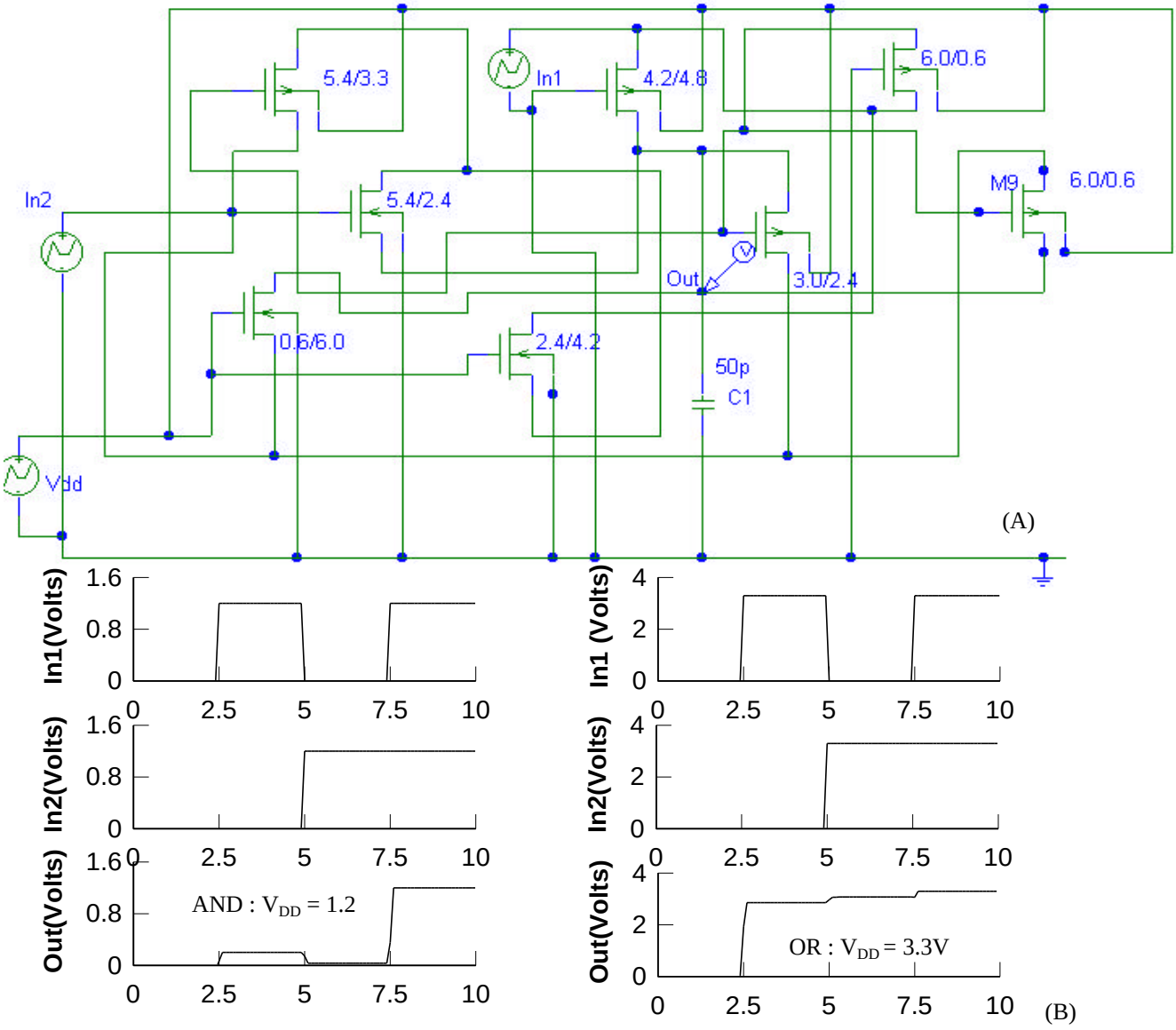

Figure 4 – Schematic of an evolved polymorphic circuit controlled by supply voltages. Circuit inputs and response for two cases, V_{DD}=1.2V (left) and V_{DD}=3.3V (right). Axis X of the graphs gives the time in milliseconds.